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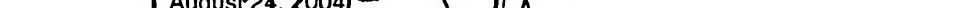
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|--|----------------------|------------------------|------------|
| <b>TRANSMITTAL<br/>FORM</b><br><i>(to be used for all correspondence after initial filing)</i> | Application Number   | 10/066,095             |            |
|  | Filing Date          | 1/31/2002              |            |
|  | First Named Inventor | Steven Teig, et al.    |            |
|  | Group Art Unit       | 2825                   |            |
|  | Examiner Name        | Brandon Bowers         |            |
| Total Number of Pages in This Submission   |                      | Attorney Docket Number | SPLX.P0074 |

**Enclosures (Check all that apply)**

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SIGNATURE OF APPLICANT ATTORNEY OR AGENT

|                            |  |
|----------------------------|--|
| Firm Or<br>Individual name | Mani Adeli, Reg. No. 39,585 of Stattler Johansen & Adeli LLP                         |
| Signature                  |  |
| Date                       | August 24, 2004  |

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| <b>Typed or printed name</b> | Mani Adeli   |             |                 |
| <b>Signature</b>             |  | <b>Date</b> | August 24, 2004 |

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



PATENT  
Docket No. SPLX.P0074

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Mani Adei

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 10/066,095

Filing Date: 1/31/2002

For: METHOD AND APPARATUS FOR  
IDENTIFYING A SET OF PATHS

Examiner: Brandon Bowers

Group Art Unit: 2825

**INFORMATION DISCLOSURE  
STATEMENT UNDER 37 C.F.R. § 1.97**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit with this Information Disclosure Statement the attached Form PTO-1449, and copies of the documents listed in the 1449 form for consideration by the Examiner. The Examiner is requested to make these documents of record. Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to

the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is submitted within three months of the application filing date or before the mailing date of a first Office Action on the merits; accordingly, no fee or separate requirements are required.

However, in the unlikely event that the Patent Office determines that additional fees, extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 50-1128** referencing **SPLX.P0074**. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: August 24, 2004

Respectfully submitted,  
By: \_\_\_\_\_  
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| Substitute for form 1449A/PTO<br><b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b><br><i>(use as many sheets as necessary)</i> |   |    |   | <b>Complete if Known</b> |                     |
| Sheet   | 1 | of | 1 | Application Number       | 10/066,095          |
|   |   |    |   | Filing Date              | 1/31/2002           |
|   |   |    |   | First Named Inventor     | Steven Teig, et al. |
|   |   |    |   | Group Art Unit           | 2825                |
|   |   |    |   | Examiner Name            | Brandon Bowers      |
|   |   |    |   | Attorney Docket Number   | SPLX.P0074          |

| <b>FOREIGN PATENT DOCUMENTS</b> |                          |  |           |                                      |  |   |                |
|---------------------------------|--------------------------|--|-----------|--------------------------------------|--|---|----------------|
| Examiner*<br>Initials           | Cite<br>No. <sup>1</sup> | Foreign Patent Document<br>Office <sup>3</sup> Number <sup>4</sup> |           | Date of<br>Publication<br>MM-DD-YYYY | Name of Patentee or<br>Applicant of Cited Document | Pages, Columns, Lines,<br>Where Relevant Passages or<br>Relevant Figures Appear | T <sup>6</sup> |
|                                 | 1.                       | JP   | 02-262354 | 10-25-1990                           | Kuribayashi, Mototaka                              |   |                |

| <b>NON PATENT LITERATURE DOCUMENTS</b> |                          |   |  |  |  |  |                |
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| Examiner*<br>Initials                  | Cite<br>No. <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. |  |  |  |  | T <sup>6</sup> |
|  | 2.                       | CHO J.D., Wiring Space and Length Estimation in Two-Dimensional Arrays, May 2000, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, VOL. 19, Iss. 5, pp. 612-615.   |  |  |  |  |                |
|  | 3.                       | CONG J. et al., DUNE – A Multilayer Gridless Routing System, May 2001, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp. 633-647.  |  |  |  |  |                |
|  | 4.                       | DION J. et al., Contour: A Tile-based Gridless Router, March 1995, Digital Western Research Laboratory, research Report 95-3, pp. 1-22.   |  |  |  |  |                |
|  | 5.                       | JUTTNER et al., "Lagrange Relaxation Based Method for the QoS Routing Problem, IEEE, Apr. 26, 2001, pp 259-268.   |  |  |  |  |                |
|  | 6.                       | SCHULZ U., Hierarchical Physical Design System, CompEuro '89, VLSI and Computer Peripherals. VSLI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks. Proceedings, 8-12 May 1989, pp. 5/20 - 5/24.                  |  |  |  |  |                |
|  | 7.                       | TSENG H-P. et al., A Gridless Multilayer Router for Standard Cell Circuits Using CTM Cells, Oct. 1999, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 18, iss. 10, pp. 1462-1479.   |  |  |  |  |                |

|                       |                    |
|-----------------------|--------------------|
| Examiner<br>Signature | Date<br>Considered |
|-----------------------|--------------------|

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